DETAILED ACTION

EXAMINER'S AMENDMENT

1. The following Examiner's Amendment to *claims 1 and 20-22* was kindly agreed upon and authorized during a telephone conversation with *Mr. Mark Beloborodov, Esq. (Registration No. 50,773)* on *15 April 2010.*

1. *(Currently Amended)* A display unit comprising:

a display including display elements which are combined into groups of display elements,

a circuit arrangement for controlling the display,

the circuit arrangement including switches and inverters which are connected in series to form a series arrangement,

each group of the groups of display elements is connected to an output of one of the inverters, and

at least one clock bus line to supply a first clock signal and a second clock signal, wherein

a first set of the switches is closed with the first clock signal when a second set of the switches is opened with the second clock signal so that after application of a third clock signal to an input of the series arrangement, at least one of the groups of display elements is activated,

wherein the display elements are arranged in N rows, and wherein

a number of transistors of the groups consists of 6N transistors for non-interlaced control of the groups ~~and 7N transistors for interlaced control of the groups~~.

20. *(Currently Amended)* The display unit of claim 1, wherein the 6N transistors comprise 4N n-transistors and 2N p-transistors~~, and wherein the 7N transistors comprise 4N n-transistors and 3N p-transistors~~.

21. *(Currently Amended)* The display unit of claim 1, wherein a number of connections to elements external to the display unit for controlling the display unit is **5** ~~[[7]]~~.

22. *(Currently Amended)* The display unit of claim 1, wherein a number of connections to elements external to the display unit for the non-interlaced control of the display unit is 5~~, and the number of connections is 7 for the interlaced control of the display~~.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

3. Applicant's election without traverse of ***Invention I (claims 1-6 and 20-22)*** in the reply filed on *12 February 2010* is acknowledged and appreciated.

4. ***Claims 12, 15, and 23-25 are withdrawn*** from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on *12 February 2010*.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. *Claims 1-6 and 20-22* are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 1 recites the limitation "*N*" (*line 15*). There is insufficient antecedent basis for this limitation in the claim.

8. The term/variable "*N*" in claim 1 (*line 15*) is a relative term which renders the claim indefinite.

The term term/variable "*N*" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

It would be unclear to one having ordinary skill in the art what the term/variable "*N*" is intended to represent.

For example, "*N*" could be meant to represent a number, size, transistor type, position, color, material, etc.

9. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

10. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. *Claims 1-6 and 20-22* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Hebiguchi (US 6,292,237 B1)*** in view of ***Reita (REITA C: "Integrated Driver Circuits for Active Matrix Liquid Crystal Displays," Vol. 14, No. 2, 1993, pages 104-114)***.

Regarding claim 1, ***Hebiguchi*** discloses a display unit [*e.g., Fig. 9A*] comprising:

a display [*e.g., Fig. 9A: matrix 41; Fig. 11*] including display elements [*e.g., Fig. 11: pixels PX(i-1, j-2), PX(i, j-2), PX(i+1, j-2), PX(i-1, j), PX(i, j), PX(i+1, j), PX(i-1, j+2), PX(i, j+2), PX(i+1, j+2), etc. -- wherein each pixel/"display element" is connected to a row of the first gate line group G1A-G480A*] which are combined into groups [*e.g., Figs. 10, 11: odd numbered rows G1A-G480A*] of display elements,

a circuit arrangement [*e.g., Fig. 10: first flip-flop group 131A-134A contained within each stage REG1-REG480 of shift register 46*] for controlling the display,

the circuit arrangement including switches [*e.g., Fig. 10: transfer gates 131A, 133A*] and inverters [*e.g., Fig. 10: inverters 132A, 134A*] which are connected in series to form a series arrangement [*e.g., Fig. 10: 131A + 132A + 133A + 134A*],

each group [*e.g., Fig. 10: each row G1a-G480a*] of the groups of display elements [*e.g., Fig. 10: each pixel PX along one of the plurality of gate line G1A-G480A*] is connected to an output of one of the inverters [*e.g., Fig. 10: output of inverter 134A*], and

at least one clock bus line [*e.g., Fig. 10: two-phase clocks CK1, CK2*] to supply a first clock signal [*e.g., Fig. 10: first phase clock CK1*] and a second clock signal [*e.g., Fig. 10: second phase clock CK2*], wherein

a first set of the switches [*e.g., Fig. 10: first transfer gates 131A*] is closed with the first clock signal [*e.g., Fig. 10: first phase clock CK1*] when a second set of the switches [*e.g., Fig. 10: first phase clock CK1*] is opened with the second clock signal [*e.g., Fig. 10: second phase clock CK2*]

so that after application of a third clock signal [*e.g., Fig. 10: start pulse SPA*] to an input of the series arrangement, at least one of the groups of display elements is activated [*e.g., Fig. 10: wherein gate lines G1a-G480a are successively activated in a progressive row-by-row sequence*], wherein

the display elements are arranged in N rows [*e.g., N = 480 rows*]

(*see the entire document, including Column 8, Line 53 - Column 9, Line 45*).

Hebiguchi does not appear to expressly disclose forming each of the *inverters* with two CMOS transistors.

However, ***Reita*** discloses an inverter [*e.g., Fig. 5(b)*] being formed by a parallel arrangement of a first p-transistor and a second n-transistor (*see the entire document, including Page 109*).

Using ***Reita's*** CMOS inverter [*e.g., Fig. 5(b)*] to form each of ***Hebiguchi's*** inverters [*e.g., Fig. 10: 132A, 134A*] would result in the instantly claimed subject matter:

a number of transistors of the groups consists of 6N transistors [*e.g., Fig. 10: 131A = 1 transistor; 132A = 2 CMOS transistors; 133A = 1 transistor; 134A = 2 CMOS transistors -- i.e., 6 transistors for each row*] for non-interlaced control of the groups [*e.g., Fig. 10: wherein gate lines G1a-G480a are successively activated in a progressive row-by-row sequence*].

Hebiguchi and ***Reita*** are analogous art, because they are from the shared inventive field of shift registers comprising inverters for driving display units.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Reita's*** CMOS inverter [*e.g., Fig. 5(b)*] to form ***Hebiguchi's*** inverters [*e.g., Fig. 10: 132A, 134A*], so as to use a commonly known and well understood inverter circuit that results in low operational power consumption.

Regarding claim 2, ***Hebiguchi*** discloses a carrier [*e.g., Fig. 9B: 40*] on which the display elements are arranged in a display field [*e.g., Fig. 9A: 41*], wherein the at least one clock bus line extends along an edge [*e.g., Fig. 9A: 46*] of the display field (*see the entire document, including Figs. 9A, 9B, 10; and Column 8, Line 53 - Column 9, Line 45*).

Regarding claim 3, ***Hebiguchi*** discloses the groups of display elements are each formed by a row or a column of a matrix display [*e.g., Fig. 10: rows G1a-G480a*] (*see the entire document, including Fig. 10; and Column 8, Line 53 - Column 9, Line 45*).

Regarding claim 4, ***Hebiguchi*** discloses each switch of the switches is formed by a first n-transistor (*see the entire document, including Fig. 10; and Column 8, Line 53 - Column 9, Line 45*).

Reita discloses each inverter of the inverters is formed by a parallel arrangement of a p-transistor and a second n-transistor (*see the entire document, including Fig. 5(b): Page 109*).

Regarding claim 5, ***Hebiguchi*** discloses the groups of display elements are connected to respective outputs of the inverters of the series arrangement (*see the entire document, including Fig. 10; and Column 8, Line 53 - Column 9, Line 45*).

Regarding claim 6, ***Hebiguchi*** discloses the groups of display elements include sampled rows or sampled columns of a matrix display (*see the entire document, including Fig. 10; and Column 8, Line 53 - Column 9, Line 45*).

Regarding claim 20, using ***Reita's*** CMOS inverter [*e.g., Fig. 5(b)*] to form each of ***Hebiguchi's*** inverters [*e.g., Fig. 10: 132A, 134A*] would result in the instantly claimed subject matter:

the 6N transistors comprise 4N n-transistors [*e.g., Fig. 10: 131A = 1 n-transistor; 132A = 1 n-transistor; 133A = 1 n-transistor; 134A = 1 n-transistor -- i.e., 4 n-transistors for each row*] and 2N p-transistors [*e.g., Fig. 10: 132A = 1 p-transistor; 134A = p n-transistor -- i.e., 2 p-transistors for each row*] (*see the entire document, including Fig. 10; and Column 8, Line 53 - Column 9, Line 45*).

Regarding claim 21, using ***Reita's*** CMOS inverter [*e.g., Fig. 5(b)*] to form each of ***Hebiguchi's*** inverters [*e.g., Fig. 10: 132A, 134A*] would result in the instantly claimed subject matter:

a number of connections [*e.g.*, ***Hebiguchi:*** *Fig. 10: CK1, CK2, SPA* + ***Reita:*** V_{DD}, *GND - - resulting in 5 external connections*] to elements external to the display unit for controlling the display unit is 5 (*see the entire document, including Column 8, Line 53 - Column 9, Line 45*).

Regarding claim 22, using ***Reita's*** CMOS inverter [*e.g., Fig. 5(b)*] to form each of ***Hebiguchi's*** inverters [*e.g., Fig. 10: 132A, 134A*] would result in the instantly claimed subject matter:

a number of connections [*e.g.*, ***Hebiguchi:*** *Fig. 10: CK1, CK2, SPA* + ***Reita:*** V_{DD}, *GND - - resulting in 5 external connections*] to elements external to the display unit for the non-interlaced control [*e.g., Fig. 10: wherein gate lines G1a-G480a are successively activated in a progressive row-by-row sequence*] of the display unit is 5 (*see the entire document, including Column 8, Line 53 - Column 9, Line 45*).

Response to Arguments

13. Applicant's arguments filed on *26 October 2009* have been fully considered but they are not persuasive.

The Applicant contends, "***Hebiguchi*** *does not disclose or suggest the present invention as recited in independent claim 1, ... amongst other patentable elements, recites (illustrative emphasis provided): wherein the display elements are arranged in N rows, and wherein a number of transistors of the groups consists of 6N transistors for non-interlaced control of the*

groups..." (see Page 11 of the Response filed on *26 October 2009*). However, the examiner respectfully disagrees.

Firstly, in response to applicant's argument that ***Hebiguchi*** does not teach *non-interlaced control of the groups*, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Secondly, ***Hebiguchi*** does teach an "*interlace scanning method*" for the entire display, including alternately driving the first set of gate lines [*Figs. 10, 11: G1a-G480a*] and then the second set of gate lines [*Figs. 10, 11: G1b-G480b*] (*e.g., see Column 9, Line 37*).

However, this "*interlace scanning method*" consists of:

(a) *successively* scanning each of the first gate lines [*Figs. 10, 11: G1a-G480a*] in a *progressive (i.e., non-interlace) row-by-row sequence*; and

(b) *successively* scanning each of the second gate lines [*Figs. 10, 11: G1b-G480b*] in a *progressive (i.e., non-interlace) row-by-row sequence.*

Moreover, for the purposes of reading on the instantly claimed subject matter, this Office action's rejections are unconcerned with ***Hebiguchi's*** second gate lines [*Figs. 10, 11: G1b-G480b*] and the second gate line pixels [*e.g., Fig. 11: pixels PX(i-1, j-1), PX(i, j-1), PX(i+1, j-1),*

PX(i-1, j+1), PX(i, j+1), PX(i+1, j+1), PX(i-1, j+3), PX(i, j+3), PX(i+1, j+3), etc. -- wherein each pixel/"display element" is connected to a row of the second gate line group G1B-G480B].

This Office action is only directed to ***Hebiguchi's*** 1st flip-flops [*Fig. 10: 131A-134A*], 1st gate line group [*Fig. 10: G1a-G1b*], and the pixels connected thereto [*e.g., Fig. 11: pixels PX(i-1, j-2), PX(i, j-2), PX(i+1, j-2), PX(i-1, j), PX(i, j), PX(i+1, j), PX(i-1, j+2), PX(i, j+2), PX(i+1, j+2), etc. -- wherein each pixel/"display element" is connected to a row of the first gate line group G1A-G480A*].

As such, ***Hebiguchi*** discloses a display [*e.g., Fig. 9A: matrix 41; Fig. 11*] including display elements [*e.g., Fig. 11: pixels PX(i-1, j-2), PX(i, j-2), PX(i+1, j-2), PX(i-1, j), PX(i, j), PX(i+1, j), PX(i-1, j+2), PX(i, j+2), PX(i+1, j+2), etc. -- wherein each pixel/"display element" is connected to a row of the first gate line group G1A-G480A -- and not connected to a row of the second gate line group G1B-G480B*] which are combined into groups of display elements [*e.g., Fig. 10: rows of pixels PX commonly connected to each gate line G1A-G480A -- and not connected to a row of the second gate line group G1B-G480B*], as instantly claimed.

Hebiguchi does not appear to expressly disclose forming each of the *inverters* with two CMOS transistors.

However, ***Reita*** discloses an inverter [*e.g., Fig. 5(b)*] being formed by a parallel arrangement of a first p-transistor and a second n-transistor (*see the entire document, including Page 109*).

Using ***Reita's*** CMOS inverter [*e.g., Fig. 5(b)*] to form each of ***Hebiguchi's*** inverters [*e.g., Fig. 10: 132A, 134A*] would result in the instantly claimed subject matter:

a number of transistors of the groups consists of 6N transistors [*e.g., Fig. 10: 131A = 1 transistor; 132A = 2 CMOS transistors; 133A = 1 transistor; 134A = 2 CMOS transistors -- i.e., 6 transistors for each row*] for non-interlaced control of the groups [*e.g., Fig. 10: wherein gate lines G1a-G480a are successively activated in a progressive row-by-row sequence*].

Applicant's arguments with respect to *claims 1-6 and 20-22* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
15 April 2010